REMARKS/ ARGUMENTS

Favorable reconsideration of this application, as presently amended and in light of the following discussion, is respectfully requested.

Claims 1-30 are pending in the present application. Claims 1-29 have been amended and Claim 30 has been added in the present response.

In the outstanding Office Action, Claims 1, 6, 14, and 19 were objected to as including informalities; Claims 11-13, and 24-29 were rejected under 37 C.F.R. §1.75 (c) as being in improper form; Claims 1-3, 6-8, 14-16, and 19-22 were rejected under non-statutory obviousness type double patenting over Takahashi et al. (U.S. Patent No. 6,658,581, herein Takahashi'581) to in light of Osborn et al. (U.S. Patent No. 6,721,892, herein Osborn), and further in light of Maskas (U.S. Patent No. 5,428,764, herein Maskas) and Takahashi et al. (U.S. Patent No. 6,993,672, herein Takahashi'672), in view of Osborn and Maskas; and Claims 1-10 and 14-23 were rejected under 35 U.S.C. §103(a) as unpatentable over Takahashi in view of Osborn in view of Maskas.

With respect to the objection to Claims 1, 6, 14, and 19 as including informalities, Claims 1, 6, 14, and 19 are amended as was suggested in the outstanding Action in order to overcome the objection. Accordingly, Applicants respectfully request the objection to Claims 1, 6, 14, and 19 be withdrawn.

With respect to the objection to Claims 11-13 and 24-29 as being in improper form, Claims 11-13 and 24-28 are amended to correct the dependency of the claims. Accordingly, Applicants respectfully request the objection to Claims 11-13 and 24-29 be withdrawn.

In response to the rejection based on the obviousness-type double patenting, submitted herewith is a Terminal Disclaimer to overcome the rejection based on U.S. Patent 6,658,581 and U.S. Patent 6,993,672 in view of U.S. Patent 6,721,892 in view of U.S. Patent

5,428,764. Applicants therefore respectfully request that the obviousness-type double patenting rejection be withdrawn.

Addressing now the rejections of Claims 1-10 and 14-23 under 35 U.S.C. § 103(a) as unpatentable over Takahashi in view of Osborn and Maskas, this rejection is respectfully traversed.

Claim 1 recites,

> A digital system that carries out digital processing in accordance with a single or a plurality of digital clock signals to perform a prescribed basic function, the digital system comprising:
>
> a plurality of delay elements provided therein each comprising a circuit element that configured to change a delay time according to a value indicated by a control signal, the circuit element inserted in each of a plurality of clock circuits that supply the clock signals, and
>
> a plurality of holding circuits configured to hold a plurality of control signals applied to the plurality of delay elements, wherein, in a state in which the digital system is supplied with power from a variable output voltage power supply apparatus, values of the plurality of control signals held by the plurality of holding circuits are changed by an external apparatus in accordance with a probabilistic search technique so that a basic function of the digital system satisfies prescribed specifications.

Claims 6, 14 and 19 recite similar features.

As is described in paragraph 0013 of the present disclosure, in the case of low electric power consumption systems including mobile telephone and other such digital systems that operate at a low supply voltage, the slow operating speed of the constituent logic elements of the system can easily give rise to disorder due to faulty timing. Thus it is necessary to adjust the timing of the system in order to achieve normal operation when using a supply voltage that is lower than usual.

In order to address at least this problem, the claimed invention describes automatically adjusting the timing of the clock signals of individual digital systems which

have supply voltages differing from the usual supply voltage. Specifically, in order to attain this adjustment, the claimed invention implements changing values of a plurality of control signals held by a plurality of holding circuits, in a state in which the digital system is supplied with power from a variable output voltage power supply apparatus, in accordance with a probabilistic search technique so that a basic function of the digital system satisfies prescribed specifications.

Takahashi describes a digital processing system for automatically adjusting a clock signal timing for each digital system.

However, as acknowledged in the outstanding Action on page 5, Takahashi does not describe or suggest that the digital system is supplied with power from a variable output voltage power supply apparatus. Nevertheless the outstanding Action relies on Osborn as curing this deficiency.

Osborn describes a dynamic performance circuit adjustment system and method to adjust the performance of logic circuits. The logic circuit performs processing operations while the dynamic performance circuit flexibly alters the voltage and frequencies of the logic circuit with respect to the task to be completed and duration of the task. Osborn discloses the object of its invention is to provide a system for adjusting performance abilities on maximum and minimum performance levels while providing power conservation during the processing step.

However, as acknowledged in the outstanding Action on page 5, neither Takahashi nor Osborn describes or suggests that values of the plurality of control signals held by the plurality of holding circuits are changed by an external apparatus in accordance with a probabilistic search technique so that a basic function of the digital system satisfies prescribed specifications. Nevertheless the outstanding Action relies on Maskas as curing this deficiency.

In Maskas, radially distributed clocking systems convert standard bus clock signals to inverted and non-inverted clocking signals in order to reduce computing system skew errors. The signal conversions require two pairs of inverted and non-inverted clocking signals where the second pair is delayed for a set time period pertaining to the first pair of clocking signals.

However, Maskas does not teach or suggest changing values of a plurality of control signals used by a variety of holding circuits where the digital system's power supply comes from an output voltage supply complying with the probabilistic search technique as suggested in Claim 1.

In other words, while Claim 1 recites that values of the plurality of control signals held by the plurality of holding circuits are changed by an external apparatus ***in accordance with a probabilistic search technique so that a basic function of the digital system satisfies prescribed specifications***, Maskas merely describes that clocking skew caused by a number of factors can be corrected. Thus, nothing in Maskas states that values of the plurality of control signals held by the plurality of holding circuits are changed by an external apparatus in accordance with a probabilistic search technique so that a basic function of the digital system satisfies prescribed specifications.

As described above, Takashi, Osborn, and Maskas each differ in teachings from those of the present invention. Further, the combination of these references does not describe or suggest changing values of a plurality of control signals held by a variety of holding circuits where the digital system's power supply comes from a variable output voltage apparatus allowing the digital system to perform basic functions according to predetermined specifications as suggested in independent Claims 1, 6, 14, and 19 of the present invention. Accordingly, Applicants respectfully submit that independent Claims 1, 6, 14, 19, and claims depending therefrom are allowable.

Consequently, in light of the above discussion and in view of the present amendments, the application is believed to be in condition for formal allowance. An early and favorable action to that effect is respectfully requested.

Respectfully submitted,

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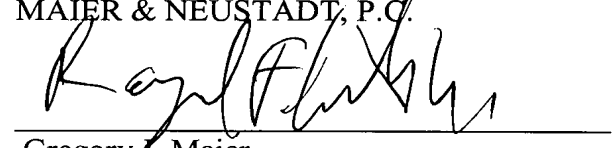

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